WHAT IS CLAIMED IS:

1. A data processor comprising:

an instruction execution pipeline comprising N processing stages;

an instruction issue unit capable of fetching into said instruction execution pipeline instructions fetched from an instruction cache associated with said data processor, each of said fetched instructions comprising from one to S syllables; and

a constant generator unit capable of receiving said fetched instruction syllables and capable of generating at least one constant operand by decoding at least one constant operand instruction comprising at least one syllable containing a K bit constant field containing K bits that represent a constant operand.

2. The data processor as set forth in Claim 1 wherein said at least one syllable of said constant operand instruction contains at least one op code field that contains at least one op code.

3. The data processor as set forth in Claim 1 wherein said constant generator unit comprises

an input data path coupled to a sign extension unit, said input data path capable of providing to said sign extension unit K bits of data that represent a short constant operand within said at least one syllable;

wherein said sign extension unit is capable of right justifying said K bits of data in an output syllable; and

an output data path coupled to said sign extension unit capable of receiving from said sign extension unit said output syllable containing said right justified K bits of data that represent said short constant operand.

4. The data processor as set forth in Claim 3 wherein said sign extension unit is capable of placing leading zeros in front of said right justified K bits when said short constant operand is positive.

5. The data processor as set forth in Claim 3 wherein said sign extension unit is capable of placing leading ones in front of said right justified K bits when said short constant operand is negative.

6. The data processor as set forth in Claim 3 wherein said constant operand instruction comprises at least one extension syllable containing a T bit constant field containing T bits of data that represent the high order bits of a long constant operand comprising T high order bits and K low order bits.

7. The data processor as set forth in Claim 6 wherein the value of K is nine and the value of T is twenty three.

8. The data processor as set forth in Claim 6 wherein said at least one extension syllable further comprises an EXT bit field containing an EXT bit for determining whether said constant operand instruction is to decode a long constant operand.

9. The data processor as set forth in Claim 6 wherein said at least one extension syllable further comprises an association bit field containing bits for determining which of two data paths to select to obtain T bits that represent the high order bits of said long constant operand.

10. The data processor as set forth in Claim 6 wherein said constant generator unit comprises

a first data path capable of receiving from said at least one extension syllable T bits of data that represent the high order bits of a long constant operand;

a second data path capable of receiving from said at least one constant operand instruction K bits of data that represent the low order bits of said long constant operand; and

a third data path capable of receiving said T bits of data from said first data path and capable of receiving said K bits of data from said second data path and capable of combining said T bits of data and said K bits of data to provide a representation of said long constant operand.

11. The data processor as set forth in Claim 10 wherein the value of K is nine and the value of T is twenty three.

12. The data processor as set forth in Claim 1 wherein said constant generator unit comprises:

a multiplexer having a first input capable of receiving from an extension syllable from a first issue lane T bits of data that represent the high order bits of a long constant operand;

said multiplexer having a second input capable of receiving from an extension syllable from a second issue lane T bits of data that represent the high order bits of a long constant operand;

said multiplexer coupled to an output data path and capable of sending to said output data path one of said T bits of data from said first issue lane and said T bits of data from said second issue lane; and

a constant generator controller coupled to said multiplexer, said constant generator controller capable of enabling said first input of said multiplexer when bits in an association bit field in said extension syllable are set equal to a first predetermined number, and said constant generator controller capable of enabling said second input of said multiplexer when said bits in said association bit field in said extension syllable are set equal to a second predetermined number.

13. The data processor as set forth in Claim 1 wherein said constant generator unit comprises:

a first input data path couple to a sign extension unit, said input data path capable of providing to said sign extension unit K bits of data that represent one of:

1) the bits of a short constant operand, and

2) the low order bits of a long constant operand;

wherein said sign extension unit is capable of right justifying said K bits of data in an output syllable;

a multiplexer having a first input coupled to the output of said sign extension unit and capable of receiving from said sign extension unit said output syllable containing said right justified K bits of data;

said multiplexer having a second input capable of receiving a combination of K bits of data and T bits of data, where said K bits of data are the low order bits of a long constant operand and where said T bits of data are the high order bits of said long constant operand; and

a constant generator controller coupled to said multiplexer, said constant generator controller capable of enabling said

first input of said multiplexer when an EXT bit in said extension syllable is set equal to zero, and said constant generator controller capable of enabling said second input of said multiplexer when said EXT bit in said extension syllable is set equal to one.

14. The data processor as set forth in Claim 13 wherein the value of K is nine and the value of T is twenty three.

15. For use in a data processor comprising an instruction execution pipeline comprising N processing stages, a method of encoding a short constant operand comprising the steps of:

receiving in a sign extender unit an input syllable that contains a K bit field containing K bits that represent a short constant operand;

selecting said K bits from said input syllable;

right justifying said K bits in an output syllable; and

sending said output syllable to an output data path.

16. The method as set forth in Claim 15 further comprising the steps of:

determining that said K bits represent a positive short constant operand; and

placing leading zeroes in the high order bits of said output syllable.

17. The method as set forth in Claim 15 further comprising the steps of:

determining that said K bits represent a negative short constant operand; and

placing leading ones in the high order bits of said output syllable.

18. For use in a data processor comprising an instruction execution pipeline comprising N processing stages, a method of encoding a long constant operand comprising the steps of:

receiving an extension syllable from a first input lane, where said extension syllable contains a T bit field containing T bits that represent the high order bits of said long constant operand;

receiving a first instruction syllable from a second input lane, where said first instruction syllable contains a K bit field containing K bits that represent the low order bits of said long constant operand;

placing said K bits on a first data path;

placing said T bits on a second data path;

combining said K bits and said T bits on a third data path where the combination of said K bits and said T bits represent said long constant operand.

19. The method as claimed in Claim 18 wherein the value of K is nine and the value of T is twenty three.

20. A method as claimed in Claim 18 further comprising the steps of:

coupling to a first input of a multiplexer a first set of T bits that represent the high order bits of said long constant operand;

coupling to a second input of said multiplexer a second set of T bits that represent the high order bits of said long constant operand;

enabling the first input of said multiplexer with a constant generator controller when an EXT bit in said extension syllable is set equal to zero;

enabling the second input of said multiplexer with said constant generator controller when said EXT bit is said extension syllable is set equal to one; and

placing the enabled set of T bits on said second data path.